Claims

1. (currently amended) A method for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:

supplying said unit of data from the source to first of said at least two destinations as a read data operation; and

supplying said unit of data to a second of said at least two destinations as a write operation.

2. (original) The method according to claim 1, wherein the source comprises a non-addressed data device.

3. (original) The method according to claim 2, wherein the source comprises a FIFO device.

4. (original) The method according to claim 1, wherein at least one of the at least two destinations comprise addressed data devices.

5. (original) The method according to claim 4, wherein the at least one destinations comprises a microprocessor.

6. (original) The method according to claim 4, wherein the at least one destinations comprises a memory storage.

7. (original) The method according to claim 4, wherein the at least one destinations comprises a SDRAM memory.

8. (currently amended) An apparatus for transferring received data in discrete units from a network, comprising:

a bus;

a media access controller for putting ones of discrete units of the received data from the network onto said bus;

a microprocessor for reading the ones of discrete units of data from said bus;

a memory for writing the ones of discrete units of data from said bus into said memory; and

a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write selected ones of discrete units of the data to the bus, said memory write said selected ones of discrete units of the data to said memory and said microprocessor read said selected ones of discrete units of the data substantially simultaneously.

9. (currently amended) An apparatus for transferring data, comprising:

a bus;

a FIFO data source connected to said bus for putting data onto said bus;

a microprocessor connected to said bus for reading the data from said bus;

a memory connected to said bus for writing the data from said bus into said memory; and

a timing controller connected to said FIFO data source, said microprocessor and said memory for controlling said FIFO data source, said microprocessor and said memory to have said FIFO data source put the data onto the bus, and for a selected quantity of data, have said memory write the selected quantity of data to said memory and said microprocessor read the selected quantity of data substantially simultaneously.

Please add new claims as follows:

10. (new) The apparatus for transferring data according to claim 9, wherein said FIFO device is a media access controller.

11. (new) The apparatus for transferring data according to claim 9, wherein said apparatus is a network test instrument and said FIFO device is a media access controller.

12. (new) The method according to claim 1, wherein said supplying as a read and write operation of said unit of data is accomplished with said unit of data being presented on said bus as a single instance.

13. (new) The method according to claim 2, wherein the source comprises a media access controller device.

14. (new) An apparatus for transferring received data in discrete units from a network according to claim 8, wherein said apparatus comprises a network test instrument.

15. (new) An apparatus for transferring received data in discrete units from a network according to claim 8, wherein said memory write of the selected quantity of data to said memory and said microprocessor read of the selected quantity of data are accomplished with said selected quantity of data being presented on said bus as a single instance.

16. (new) A method for operating a network test instrument to transfer data on a bus within said network test instrument from a media access controller at least to a processor and to a memory, separate from said processor, comprising the steps of:

supplying said data from the media access controller to said processor as a read data operation performed by said processor; and

supplying said data to said memory as a write operation,

wherein said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus.

17. (new) The method for operating a network test instrument according to claim 16, further comprising the steps of:

determining whether the data currently transferred to said memory is to be retained before a next data is transferred said memory, and if said data currently transferred is to be retained, modifying a next data write address location so that a next data does not overwrite the data currently transferred, and otherwise,

if said data currently transferred is not to be retained in said memory, keeping the next data write address as a current data write address value so that the next data is written over the data currently transferred.

18. (new) The method for transferring according to claim 7, further comprising the steps of:

determining whether the unit of data currently transferred to said SDRAM is to be retained before a next unit of data is transferred said SDRAM and if said unit of data currently transferred is to be retained, modifying a next data write address location so that a next unit of data does not overwrite the unit of data currently transferred, and otherwise, if said unit of data currently transferred is not to be retained in said SDRAM, keeping the next data write address as a current data write address value so that the next unit of data is written over the unit of data currently transferred.

19. (new) The method for transferring according to claim 1, wherein said unit of data comprises a word.